PAPER Special Section on Analog Circuits and Related SoC Integration Technologies

Analysis of CMOS Transconductance Amplifiers for Sampling Mixers

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SUMMARY In this paper the transfer function of a system with windowed current integration is discussed. This kind of integration is usually used in a sampling mixer and the current is generated by a transconductance amplifier (TA). The parasitic capacitance (C_p) and the output resistance of the TA ($R_{o,TA}$) before the sampling mixer heavily affect the performance. Calculations based on a model including the parasitic capacitance and the output resistance of the TA is carried out. Calculation results show that due to the parasitic capacitance, a notch at the sampling frequency appears, which is very harmful because it causes the gain near the sampling frequency to decrease greatly. The output resistance of the TA makes the depth of the notches shallow and decreases the gain near the sampling frequency. To suppress the effect of C_p and $R_{o,TA}$, an operational amplifier is introduced in parallel with the sampling capacitance (C_s). Simulation results show that there is a 17 dB gain increase while C_s is 1 pF, g_m is 9 mS, N is 8 with a clock rate of 800 MHz.

key words: *Windowed integration, moving average, transconductance amplifier, sampling mixer*

1. Introduction

The diversity of wireless standards calls for a universal solution for the receiver and transmitter to save cost. Recently software-defined radio (SDR) is becoming a good choice as it can tune to any frequency band, select any reasonable channel bandwidth, and detect any known modulation [1]. A windowed integration sampler with embedded filter function is usually used in SDR. In this kind of sampler, instead of tracking the signal voltage, current integration on a capacitance in a given time window is performed ; the integrated charge is accumulated on the capacitance; and after integrating over N cycles the capacitor is disconnected and the accumulated charge is transferred to the next stage. A transconductance amplifier (TA) before the sampler is needed to convert the voltage of an RF signal to a current (Fig. 1). This work is about the TA and the sampling mixer.

The ideal filter functions have been discussed in many papers [2]–[4]. However, as far as we know, there is no paper which discusses the transfer function including the parasitic capacitance and the output resistance. When the sampling capacitance is of a small value, the parasitic capacitance and the output resistance of the TA heavily affect the performance of the filters. So it is of interest to calculate the voltage transfer function considering the TA's parasitic capacitance and output resistance.

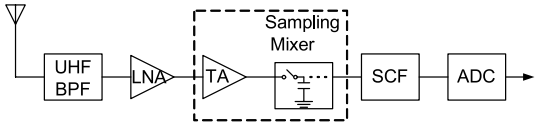

Fig. 1 Block diagram of a software-defined radio receiver.

This paper is structured as follows: Sect. 2 describes the voltage transfer function based on the ideal model of the TA and the sampling capacitance. The calculation results based on the proposed model are given in Sect. 3. The circuit design and simulation results are shown in Sect. 4. Section 5 presents the conclusions.

2. The Voltage Transfer Function Based on the Ideal Model of a TA and a Sampling Capacitor

A sample-and-hold (S/H) circuit based on current integration in a given time window is valuable for sampling narrow band signals [2], [5]. In this S/H, the RF voltage signal with a frequency f_0 is converted by a tranconznsh1991@hotmail.com ductor (g_m) to current, and integrated on a capacitance (C_s) over one clock period. Figure 2(a) shows the model for a TA and a sampling capacitance. Assuming the input RF signal is $v_{in}e^{j\omega t}$, the voltage transfer function from the input voltage (v_s) of the TA to the output voltage (v_{C_s}) of a windowed integrator is given by (1) and plotted in Fig. 3.

$$\left|\frac{v_{C_s}}{v_s}\right| = \left|\frac{g_m T_{on}}{C_s}\frac{\sin\left(\frac{\omega T_{on}}{2}\right)}{\left(\frac{\omega T_{on}}{2}\right)}\right| \tag{1}$$

where T_{on} is the pulse width of the sampling period and C_s is the sampling capacitance. As can be seen in Fig. 3, the transfer function forms a low pass filter with notches at the integer multiples of f_s. The gain and 3 dB pass band will change with the integration time window.

If the input RF signal is synchronous and in phase with the local oscillating frequency f_0, and T_{on} is half of the sampling period, the voltage gain is expressed as

$$\left|\frac{v_{C_s}}{v_s}\right| = \frac{g_m}{\pi f_0 C_s} \tag{2}$$

Without changing the sampling capacitor, integrating over N sampling cycles realizes a moving average operation and performs a finite-impulse response (FIR). The transfer

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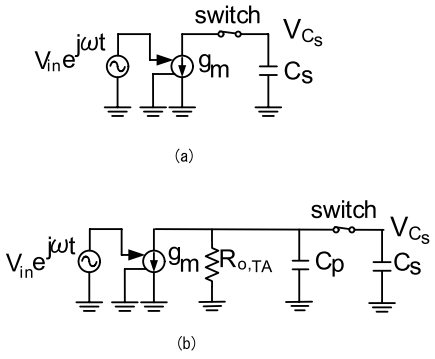


Fig. 2 Model of a TA and a sampling capacitor. (a) Ideal. (b) With TA's parasitic capacitance and output resistance.

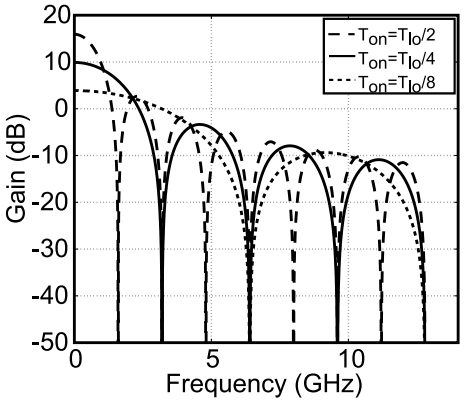


Fig. 3 Windowed-integration frequency response at a clock rate of 800 MHz.

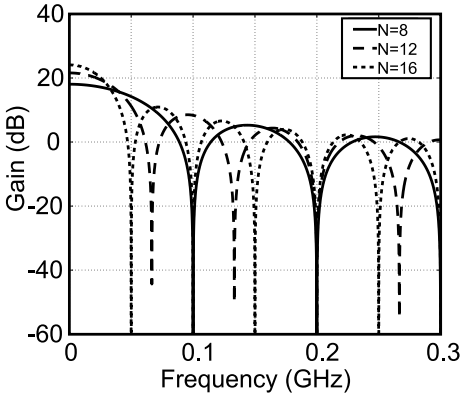


Fig. 4 Frequency response of the moving average operation at a clock rate of 800 MHz.

function of the charge moving average process is expressed as

$$|w_i| = \sum_{l=0}^{N-1} u_{i-l} \Rightarrow |F_{\mathrm{Sinc}}(\omega)| = \left| \frac{\sin\left(\frac{N\omega T_0}{2}\right)}{\sin\left(\frac{\omega T_0}{2}\right)} \right| \tag{3}$$

where u_i is the ith RF charge sample of the input current, w_i is the ith accumulated charge, T_0 is the sampling period and N is the period number [3]. The frequency response is plotted in Fig. 4 for $N = 8, 12, 16$ with a sampling frequency of 800 MHz. If the input RF signal is synchronous with the local oscillating frequency, the voltage gain of the moving average operation is equal to N.

However, in reality, due to the parasitic capacitance at the output node and the output resistance of the TA, the gain of the charge integration and moving average operation decreases and the depth of the notches becomes shallower. The detailed analysis is performed in the next section.

3. Calculation Results Based on the Proposed Model

In this section, the voltage transfer function of the charge integration and the moving average operation is calculated with the consideration of the parasitics of the TA. The proposed model is illustrated in Fig. 2(b), where C_p is the parasitic capacitance, $R_{\mathrm{o,TA}}$ is the output resistance of the TA, and C_s is the sampling capacitance. The parasitic parameters of the sampling switch are not considered here.

3.1 Charge Integration

As described in section two, a transcondutor and a sampler can realize charge integration. Based on the proposed model, the transfer function from the input current i_s to the output charge on C_s through current integration in a sampling period is expressed by

$$\begin{aligned}\left|\frac{Q_{C_\mathrm{s}}}{i_\mathrm{s}}\right| = \Bigg| & \frac{C_\mathrm{s}}{\frac{1}{R_{\mathrm{o,TA}}} + j\omega(C_\mathrm{s}+C_\mathrm{p})} \\ & \cdot \left(e^{j\omega(T_0+T_{\mathrm{on}})} - e^{j\omega T_0} e^{-\frac{T_{\mathrm{on}}}{R_{\mathrm{o,TA}}(C_\mathrm{s}+C_\mathrm{p})}}\right) \\ & + \frac{C_\mathrm{s}}{\frac{1}{R_{\mathrm{o,TA}}} + j\omega C_\mathrm{p}} \frac{C_\mathrm{p}}{C_\mathrm{s}+C_\mathrm{p}} \\ & \cdot \left(e^{j\omega T_0} - e^{j\omega(T_0-T_{\mathrm{off}})} e^{-\frac{T_{\mathrm{off}}}{R_{\mathrm{o,TA}}C_\mathrm{p}}}\right)\Bigg|\end{aligned} \tag{4}$$

where $T_{\mathrm{off}} = T_0 - T_{\mathrm{on}}$ and Q_{C_s} is the charge accumulated on C_s. The first item in (4) describes the charge accumulated on C_s when the switch is on. The second item in (4) presents the contribution of the charge accumulated on C_p while the switch is off and it is redistributed between C_s and C_p when the switch is turned on. The factors $e^{-\frac{T_{\mathrm{on}}}{R(C_\mathrm{s}+C_\mathrm{p})}}$ and $e^{-\frac{T_{\mathrm{off}}}{RC_\mathrm{p}}}$ represent the discharge through $R_{\mathrm{o,TA}}$ during the integration.

The voltage transfer function from the input voltage of the TA to the output voltage on the capacitor can be calculated from (4) and is given by (5). The result is consistent with (1), for $R_{\mathrm{o,TA}} \to \infty$ and $C_\mathrm{p} = 0$ (1) and (5) are identical. This can be shown clearly by expanding (5) as is done in the Appendix.

$$\begin{aligned}\left|\frac{v_{C_\mathrm{s}}}{v_\mathrm{s}}\right| &= \left|\frac{Q_{C_\mathrm{s}}}{i_\mathrm{s}}\right| \cdot \left|\frac{g_\mathrm{m}}{C_\mathrm{s}}\right| \\ &= \left|\frac{g_\mathrm{m}}{\frac{1}{R_{\mathrm{o,TA}}} + j\omega(C_\mathrm{s}+C_\mathrm{p})}\right|\end{aligned}$$

$$\cdot\left(e^{j\omega(T_0+T_{on})}-e^{j\omega T_0}e^{-\frac{T_{on}}{R_{o,TA}(C_s+C_p)}}\right)$$
$$+\frac{g_m}{\frac{1}{R_{o,TA}}+j\omega C_p}\frac{C_p}{C_s+C_p} \quad (5)$$
$$\cdot\left(e^{j\omega T_0}-e^{j\omega(T_0-T_{off})}e^{-\frac{T_{off}}{R_{o,TA}C_p}}\right)\Bigg|$$

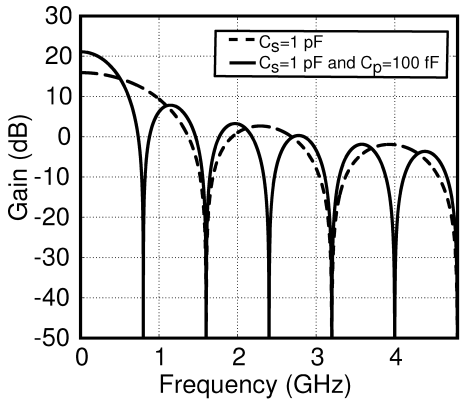
If we only consider the effect of the parasitic capacitance, for $R_{o,TA}\to\infty$, (5) is simplified to (6) and plotted in Fig. 5(a) at a half_rectified clock rate of 800 MHz. As can be seen in Fig. 5(a), comparing with the plot of the ideal case, additional notches appear at f_0 and its odd multiples due to the parasitic capacitance. It is easy to understand this result if we consider the case that the RF signal is synchronous and in phase with the sampling frequency. When the sampling switch is on, C_s and C_p will integrate charge with the same polarity at the same time. However, when the sampling switch is off, the charge on C_s will be held but C_p will continue accumulating charge with opposite polarity. And no matter how large is C_p it will integrate the same quantity as the charge integrated by C_s and C_p when the switch is on. When the switch is on in the next cycle, the charge will redistribute between C_s and C_p to make the voltage on C_s and C_p equal, which causes the charge on C_s to be neutralized and to form a notch at the sampling frequency. Because the RF signal is near the sampling frequency, the notch at f_0 turns out to be very harmful.

$$\left|\frac{v_{C_s}}{v_s}\right|=\left|\frac{g_mT_0}{(C_s+C_p)}\frac{\sin\left(\frac{\omega T_0}{2}\right)}{\left(\frac{\omega T_0}{2}\right)}\right| \quad (6)$$

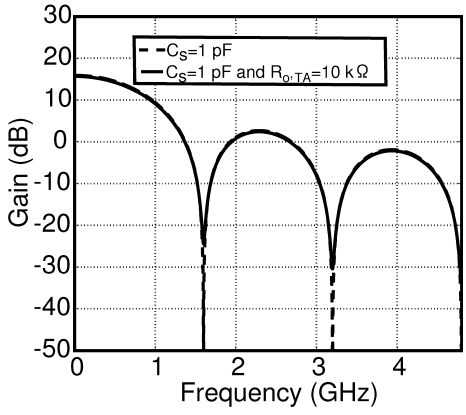
For $C_p = 0$, the effect of $R_{o,TA}$ can be derived from (5), which is given by (7) and is plotted in Fig. 5(b). Figure 5(b) shows that the gain slightly decreases because of the output resistance with a value of 10 kΩ, but the notches become greatly shallower.

$$\left|\frac{v_{C_s}}{v_s}\right|=\frac{g_m}{\sqrt{\left(\frac{1}{R_{o,TA}}\right)^2+(\omega C_s)^2}}$$
$$\cdot\sqrt{\left(1-e^{-\frac{T_{on}}{R_{o,TA}C_s}}\right)^2+4\sin^2\left(\frac{\omega T_{on}}{2}\right)e^{-\frac{T_{on}}{R_{o,TA}C_s}}} \quad (7)$$

The transfer function plotted in Fig. 5(c), as a result of both $R_{o,TA}$ and C_p, shows that the notches become shallower. The merit is that the gain near the sampling frequency increases greatly compared to the result when only C_p is considered, but still 15 dB lower than the ideal one, for $C_s = 1$ pF, $R_{o,TA} = 10$ kΩ and $C_p = 100$ fF. The reason is evident, part of the current flows through $R_{o,TA}$, therefore the charge accumulated on C_p decreases when the switch is off.



(a)



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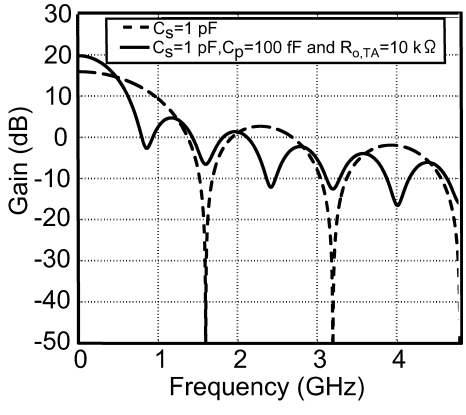


(c)

Fig. 5 The comparison of the calculated windowed integration frequency response at a clock rate of 800 MHz, g_m of 10 mS and pulse width equals to half of the clock period. (a) C_s and C_s with C_p. (b) C_s and C_s with $R_{o,TA}$. (c) C_s and C_s with C_s and $R_{o,TA}$.

3.2 Moving Average

As we have already shown in the ideal case the gain of the moving average is equal to *N*. But due to the parasitic parameters, the charge accumulated on the sampling capacitor C_s will leak through $R_{o,TA}$. This phenomenon is shown in

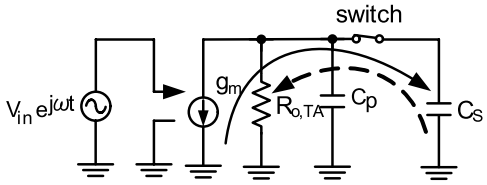


Fig. 6 Charge leakage model.

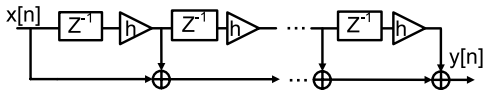


Fig. 7 Moving average model with the consideration of the parasitic parameters.

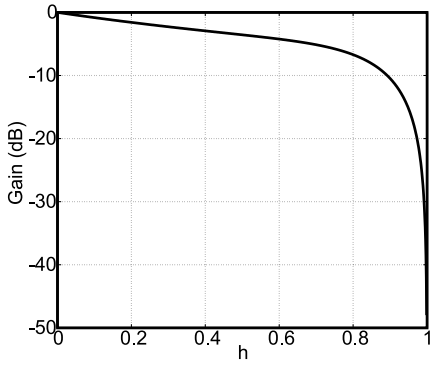


Fig. 8 Depth of the notch at half of a clock rate of 800 MHz.

Fig. 6. A model in Fig. 7 is proposed to describe this phenomenon. The transfer function of the charge moving average operation with the consideration of C_s and $R_{o,TA}$ is calculated and expressed in (8).

$$|F_{sinc}(\omega)| = \sum_{m=0}^{N-1} (hZ^{-1})^m = \sqrt{\frac{1 + h^{2N} - 2h^N \cos(N\omega T_0)}{1 + h^2 - 2h\cos(\omega T_0)}} \tag{8}$$

where

$$h = \frac{C_p e^{-\frac{T_{off}}{R_{o,TA}C_p}} + C_s}{C_s + C_p} e^{-\frac{T_{on}}{R_{o,TA}(C_s+C_p)}} \tag{9}$$

The parameter h expressed in (9) is the attenuation parameter due to the parasitics. From (9) it can be seen that h is affected by the integrating time, the sampling period, the parasitic capacitance and the output resistance of the TA. The depth of the notches in the moving average transfer function is plotted in Fig. 8 with h as a parameter; The depth of the notch becomes shallower when h decreases as can be seen in Fig. 8. For $C_p = 0$, h becomes

$$h = e^{-\frac{T_{on}}{R_{o,TA}C_s}} \tag{10}$$

For $R_{o,TA} \to \infty$ and independent of C_p, $h = 1$, which means

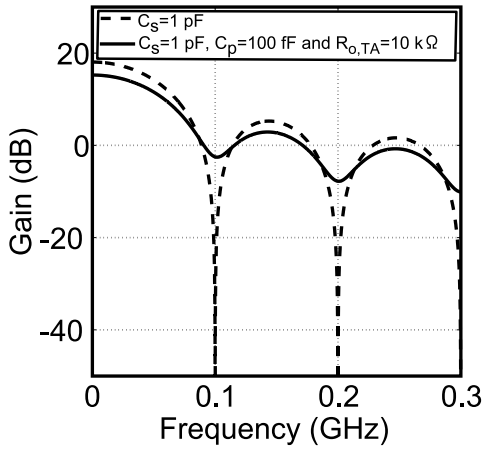


Fig. 9 Moving average with the consideration of the parasitic parameters.

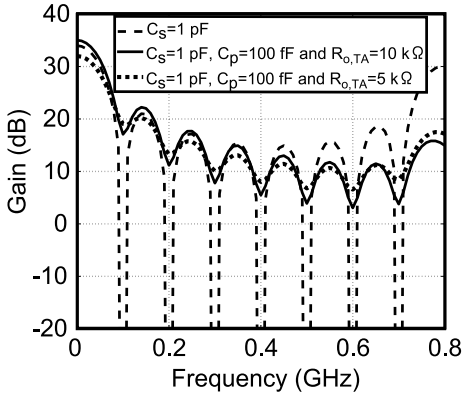


Fig. 10 The whole transfer function at a clock rate of 800 MHz.

C_p alone will not affect the depth of the notches of the moving average transfer function. The effect of $R_{o,TA}$ and C_p on the transfer function is plotted in Fig. 9.

3.3 The Whole Transfer Function

The comparison of the whole transfer function including windowed integration and moving average is carried out for different conditions and the results are plotted in Fig. 10. As illustrated in Fig. 10, the gain near the sampling frequency decreases 14 dB for $C_p = 100$ fF and $R_{o,TA} = 10$ kΩ. To some extent, decreasing $R_{o,TA}$ will increase the gain but will make the notches shallower. There is a trade-off between the depth of the notch and the gain near the sampling frequency with respect to the output resistance of the TA.

To verify the calculation result, a Spectre RF simulation based on the proposed model (see Fig. 2(b)) is implemented in the frequency range from 500 MHz to 1.1 GHz. Fig. 11 shows that the simulation and calculation result have a good match.

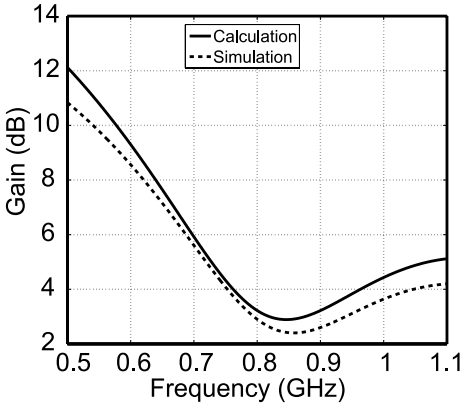


Fig. 11 The comparison between the simulation and calculation result by using the model in Fig. 2(b) while $C_s = 1\,\text{pF}$, $C_p = 100\,\text{fF}$, $R_{o,TA} = 10\,\text{k}\Omega$, $g_m = 10\,\text{mS}$ and $T_{on} = 200\,\text{ps}$.

4. TA Design

Based on the calculation result in Sect. 3, two kinds of circuits shown in Fig. 12 are analyzed and compared. The two-phase topology (Fig. 12(a)) is used in [1], [4]. In Fig. 12(a) *LO*1 and *LO*2 are two-phase non-overlapping clocks. Φ1 and Φ2 alternately switch on over N sampling clock cycles. On each side of the pseudo-differential architecture, two sampling capacitors are alternately connected to the TA. While the One connected to the TA is accumulating charge, the second will dump the accumulated charge to the following stage.

The voltage transfer function of an ideal two-phase topology is given by

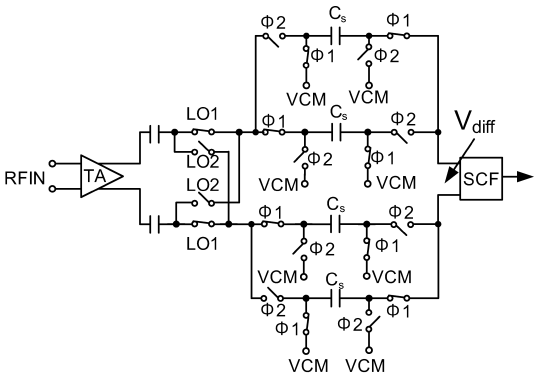
$$\left|\frac{v_{\text{diff}}}{v_s}\right| = 2\left|\frac{g_m T_{on}}{C_s}\frac{\sin\left(\frac{\omega T_{on}}{2}\right)}{\left(\frac{\omega T_{on}}{2}\right)}\right| \cdot \left|\sin\frac{\omega T_0}{4}\right| \tag{11}$$

where v_{diff} is the differential voltage of the IF signal. If the input RF signal is synchronous and in phase with the local oscillation frequency f_0, and T_{on} is half of the sampling period, the voltage gain is expressed as

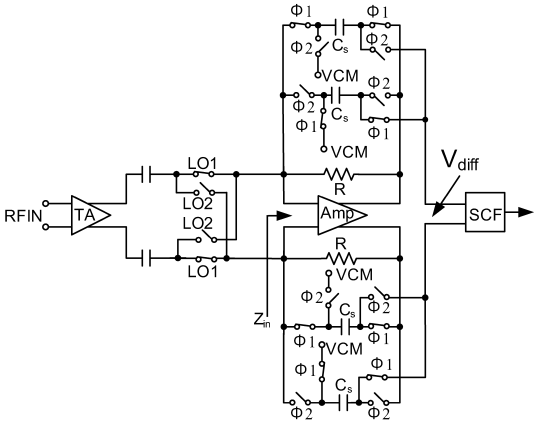
$$\left|\frac{v_{\text{diff}}}{v_s}\right| = \frac{2g_m}{\pi f_0 C_s} \tag{12}$$

We can see that the gain is twice as large as that of Fig. 2(a). However, a large capacitance is also needed in this kind of topology (about 15.5 pF used in [4]). When the sampling capacitance is small, the charge accumulated on the parasitic capacitance will still cause a problem when the switch is toggled on. The gain decreases greatly. To suppress the effect further, an operational amplifier is introduced in parallel to the sampling capacitor (Fig. 12(b)). The half-sided small signal equivalent circuit is shown in Fig. 12(c). The impedance seen at the input of the amplifier is

$$Z_{in}(f) = \frac{2}{1 + A(f)}\frac{R}{1 + sRC_s} \tag{13}$$



(a)



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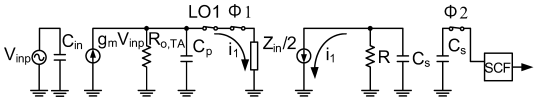

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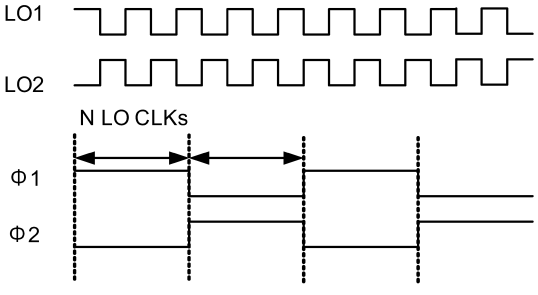

(d)

Fig. 12 TA and sampling mixer. (a) two-phase topology. (b) the proposed circuit. (c) The small signal equivalent circuit of (b). (d) the clock in (a) and (b).

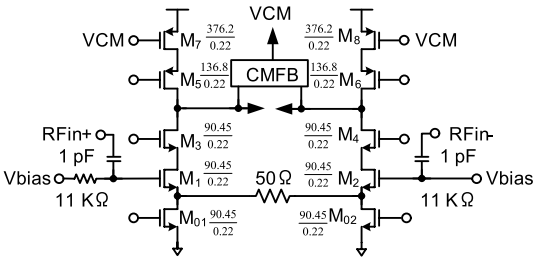

Fig. 13 TA circuit.

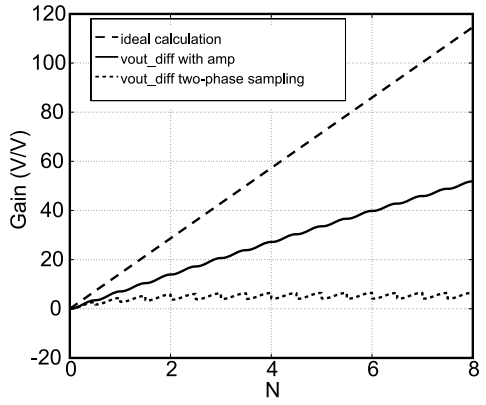

Fig. 14 Simulation results over *N*th integration.

where $A(f)$ is the open loop gain of the operational amplifier. Z_{in} is low in low frequency where $A(f)$ is high. Because the load impedance is low as can be seen in Fig. 12(c), less current will flow through the parasitic capacitance C_{p}, which means less charge will be accumulated on C_{p}. When the switch is toggled on, the effect of the charge redistribution will become smaller.

In Fig. 12(b), the fully differential amplifier with a *RC* feedback forms a low–pass filter. Only the fundamental component of the square wave of the sampling signal is considered. The conversion current gain of the fundamental component is equal to $\frac{2}{\pi}$. Therefore, the voltage transfer function from the input voltage to the output voltage of the amplifier is expressed as

$$\begin{aligned}\left|\frac{v_{\text{diff}}}{v_{\text{s}}}\right| &= \left|g_{\text{m}}\frac{2}{\pi}\frac{A(f)}{1+A(f)}\frac{R}{1+sRC_{\text{s}}}\right| \\ &\approx \left|g_{\text{m}}\frac{2}{\pi}\frac{R}{1+sRC_{\text{s}}}\right|\end{aligned} \tag{14}$$

The circuit of the TA is shown in Fig. 13. The telescopic topology is chosen for its low noise performance. A 50 Ω degeneration resistance provides high linearity. The simulated transconductance of the TA is 9.37 mS. The simulation result of the output resistance of the TA is 2.239 kΩ and the parasitic capacitance is 0.517 pF.

Figure 14 shows the simulation result. With the operational amplifier, which has an open loop gain of 40 dB, a 17 dB gain increase is achieved while $C_{\text{s}} = 1$ pF, $g_{\text{m}} = 9$ mS and $N = 8$ with a clock rate of 800 MHz.

5. Conclusion

The transfer function from the input voltage of the TA to the output voltage of a windowed integrator is calculated and simulated with the presence of the TA's parasitic capacitance and output resistance. Calculation results show that due to the parasitic capacitance, a notch at the sampling frequency appears, which is very harmful because it causes the gain near the sampling frequency to decrease greatly. The output resistance of the TA makes the depth of the notches shallow and decreases the gain near the sampling frequency. To suppress the effect of C_{p} and $R_{\text{o,TA}}$, an ideal operational amplifier with a 40 dB open loop gain is inserted in parallel with the sampling capacitance. Simulation results show there is a 17 dB gain increase while $C_{\text{s}} = 1$ pF, $g_{\text{m}} = 9$ mS and $N = 8$ with a clock rate of 800 MHz.

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Appendix

In this appendix, the voltage transfer function is expanded.

$$\begin{aligned}\left|\frac{v_{C_{\text{s}}}}{v_{\text{s}}}\right| = \Bigg|&\frac{g_{\text{m}}}{\frac{1}{R_{\text{o,TA}}}+j\omega(C_{\text{s}}+C_{\text{p}})}\left(e^{j\omega(T_0+T_{\text{on}})}-e^{j\omega T_0}e^{-\frac{T_{\text{on}}}{R_{\text{o,TA}}(C_{\text{s}}+C_{\text{p}})}}\right) \\ &+\frac{g_{\text{m}}}{\frac{1}{R_{\text{o,TA}}}+j\omega C_{\text{p}}}\frac{C_{\text{p}}}{C_{\text{s}}+C_{\text{p}}}\left(e^{j\omega T_0}-e^{j\omega(T_0-T_{\text{off}})}e^{-\frac{T_{\text{off}}}{R_{\text{o,TA}}C_{\text{p}}}}\right)\Bigg|\end{aligned} \tag{A·1}$$

Using $e^{jx} = \cos x + j \sin x$, $e^{j\omega(T_0+T_{on})}$, $e^{j\omega T_0}$ and $e^{j\omega(T_0-T_{off})}$ can be substituted with the corresponding cos and $j$sin parts. (A· 1) can be expanded and the like terms are combined. Finally, we can get the following expression.

$$\left|\frac{v_{C_s}}{v_s}\right| = g_m \sqrt{U + V + W + X} \quad (A\cdot 2)$$

The terms U, V, W and X are expressed as

$$U = A^2\left(1 + e^{-\frac{2T_{on}}{R_{o,TA}(C_s+C_p)}} - 2\cos(\omega T_{on}) e^{-\frac{T_{on}}{R_{o,TA}(C_s+C_p)}}\right) \quad (A\cdot 3)$$

$$V = (BC)^2\left(1 + e^{-\frac{2T_{off}}{R_{o,TA}C_p}} - 2\cos(\omega T_{off}) e^{-\frac{T_{off}}{R_{o,TA}C_p}}\right) \quad (A\cdot 4)$$

$$\begin{aligned} W = 2(AB)^2 CD\Big(&\cos(\omega T_{on}) - e^{-\frac{T_{on}}{R_{o,TA}(C_s+C_p)}} \\ &- e^{-\frac{T_{off}}{R_{o,TA}C_p}}\cos(\omega T_0) \\ &+ e^{-\frac{T_{on}}{R_{o,TA}(C_s+C_p)}-\frac{T_{off}}{R_{o,TA}C_p}}\cos(\omega T_{off})\Big) \end{aligned} \quad (A\cdot 5)$$

$$\begin{aligned} X = 2(AB)^2 CE\Big(&\sin(\omega T_{on}) - e^{-\frac{T_{off}}{R_{o,TA}C_p}}\sin(\omega T_0) \\ &+ e^{-\frac{T_{on}}{R_{o,TA}(C_s+C_p)}-\frac{T_{off}}{R_{o,TA}C_p}}\sin(\omega T_{off})\Big) \end{aligned} \quad (A\cdot 6)$$

Where the terms A, B, C, D and E are defined as

$$A = \frac{1}{\sqrt{\left(\frac{1}{R_{o,TA}}\right)^2 + \left(\omega(C_s + C_p)\right)^2}} \quad (A\cdot 7)$$

$$B = \frac{1}{\sqrt{\left(\frac{1}{R_{o,TA}}\right)^2 + \left(\omega C_p\right)^2}} \quad (A\cdot 8)$$

$$C = \frac{C_p}{C_s + C_p} \quad (A\cdot 9)$$

$$D = \left(\frac{1}{R_{o,TA}}\right)^2 + \omega^2(C_s + C_p)C_p \quad (A\cdot 10)$$

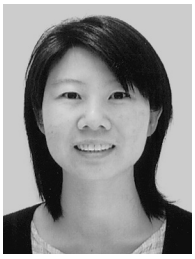
$$E = \frac{\omega C_s}{R_{o,TA}} \quad (A\cdot 11)$$

For $R_{o,TA} \to \infty$ and C_p is zero, it is easy to get that U is equal to $4(\sin\frac{\omega T_{on}}{2})^2/(\omega C_s)^2$, V, W and X are equal to zero.

Therefore,

$$\left|\frac{v_{C_s}}{v_s}\right| = \left|\frac{g_m T_{on}}{C_s}\frac{\sin\left(\frac{\omega T_{on}}{2}\right)}{\left(\frac{\omega T_{on}}{2}\right)}\right| \quad (A\cdot 12)$$

It is the same with the formula calculated from the ideal model.



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